curing and cross-linking said photosensitive polyimide thereby protecting the underlying circuitry, said curing and cross-linking of said photosensitive polyimide to take place after said etching of said passivation layer.

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REMARKS

Examiner Nema O. Berezny is thanked for thoroughly examining the Prior Art.

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

The invention teaches the deposition of a pattern of interconnecting lines and bond pads. Passivation layers are deposited over this metal pattern. A layer of photosensitive polyimide is deposited over the passivation layers. This layer of photosensitive polyimide is patterned, exposed and developed, the passivation layer is patterned and etched to expose the underlying bonding pads. The remaining polyimide is cured and cross-linked and remains in place to serve as a buffer during further device packaging.

## Specification

Reconsideration of the objection to the specification under 35 U.S.C. 132 because it introduces new matter into the disclosure is respectfully requested based on the following.

The amendment filed on 5-21-02 has been cancelled.

In light of the foregoing response, applicant respectfully requests that the Examiner's objection to the specification under 35 U.S.C. 132 be withdrawn.

## Claim rejections - 35 U.S.C. § 112

Reconsideration of the rejection of claims 1-25 and 27-30 under 35 U.S.C 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention is respectfully requested based on the following.

Claims 1, 8, 15-18 and 20 have been amended by removing any reference to "ultra-small spacing technologies", "eliminate any detrimental effect" and "adjacent" from these claims, thus removing Examiner's objection.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 1-25 and 27-30 under 35 U.S.C 112, first paragraph, be withdrawn.

Claim rejections - 35 U.S.C. § 103

Reconsideration of the rejection of claims 1-25 and 27-30 under 35 U.S.C 103(a) as being unpatentable over Dass et al. (US Patent 6,143,668) in view of Fu et al. (US Patent (5,807,787) is respectfully requested based on the following.

Dass et al. starts with a surface over which a bonding pad is provided. No pattern of metal interconnect lines has been created over the substrate used by Dass et al. The invention addresses a surface over which interconnect lines are created adjacent to a bond pad, allowing the creation of an opening to the bond pad while adjacent layers of interconnect are protected from etching effects. Dass et al. therefore does not provide for

the problem of surface damage to the passivation layer of interconnecting metal lines. Dass et al. has not addressed the occurrence of keyholes between closely spaced layers of interconnect metal.

The instant invention:

- starts with the surface of a semiconductor substrate, over which a pattern of metal has been created, including interconnect lines and bonding pads
- a first and second layer of passivation are consecutively deposited
- a thick layer of polyimide is deposited over the surface of the second layer of passivation
- the thick layer of polyimide is patterned and etched creating openings in the layer overlying the surface of the bonding pads, leaving the polyimide in place above the interconnect line pattern,
- the layers of passivation are etched, exposing the surface of the bonding pads, and
- the thick layer of polyimide is cured and cross-linked in order to provide improved protection for the interconnect metal.

Since Dass et al. does not provide for a thick layer of polyimide overlying interconnect traces Dass et al. also does not provide for protection of the passivation film (by the thick layer of polyimide) that remains in place above the interconnecting lines.

The method that is provided by Dass et al. addresses problems that are experienced with a passive scrub cantilever needle probe card and the scrubbing process, problems that become particularly acute for smaller contact pad pitch for contact pads that are used for, testing or probing of wafers. The pads that are therefore created by Dass et al. are wafer contact pads for testing purposes having a pitch of 80 microns.

Fu et al. addresses only bond pads, the instant invention addresses bonding pads that are provided on the surface of a substrate concurrent with interconnect lines. The difference is significant since, in forming a thick layer of passivation (for improved protection of the underlying components) in the era of sub-micron devices and the therewith used closely spaced interconnect lines, keyholes between interconnect lines are a problem since the thick layer of passivation (typically deposited by depositing two layers of passivation) does not readily penetrate between narrowly spaced adjacent interconnect

lines. For a typical process of etching (a passivation layer in order to expose a bonding pad), photoresist is used which, where keyholes are present (that is most typically between adjacent interconnect traces), penetrates the keyholes and, during subsequent high temperature processing, violently reacts to the high temperatures and "explodes" from the keyholes, causing significant disturbance to the process of device formation. This is to be prevented, the present invention prevents this by using a thick layer of polyimide whereby the polyimide readily penetrates any keyholes that may have formed between adjacent, closely spaced interconnect lines. With the invention, bond pads can be created without incurring processing damage by photoresist remnants that in conventional processing penetrates into keyholes between closely spaced interconnect lines.

Fu et al. deposit a layer of passivation and etch this layer (exposing the surface of the bonding pad) before depositing a layer of polyimide. The instant invention deposits the (two layers of) passivation over which the layer of polyimide is deposited. After these layers have been deposited, the polyimide is etched after which the layer of passivation is etched. The difference in sequence is significant because the instant invention first provides protection to the interconnect lines after which a bonding pad is created. Fu et al. create a bonding

pad by first creating an opening in the layer of passivation (exposing the bonding pad) after which a layer of polyimide is deposited. The layer of polyimide contacts the surface of the bonding pad, the layer of polyimide is etched again exposing the bonding pad. The etch of the polyimide leaves polyimide in place over the surface of the bonding pad (Fu et al., col. 6, line 1 e.a.) which is further removed with the additional step of oxide ashing (Fu et al, see table in col. 6, lines 6-14).

What makes the instant invention unique and therefore patentable over Dass et al. in view of Fu et al. is that neither one of these two inventions addresses the creation of a bond pad that has been provided over a semiconductor surface over which a network of interconnect traces has also has been provided. The bond pad can be accessed (exposed), leaving the interconnect traces covered and protected. Prior art processing required, in order to achieve this objective, the application of layers of photoresist with the potential of forming deposits of photoresist in keyholes between adjacent layers of interconnect traces, leading to the (potentially catastrophic) results that have been highlighted above. The invention eliminates negative effects previously created in exposing a bond pad, pad 14, Fig. 9 of the invention, which is created on a surface over which

also interconnect traces, lines 12, Fig. 9, have been created, as further specified in claims 1 and 20 of the invention.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 1-25 and 27-30 under 35 U.S.C 103(a) as being unpatentable over Dass et al. (US Patent 6,143,668) in view of Fu et al. (US Patent (5,807,787) be withdrawn.

Other Considerations

No new independent or dependent claims have been written as a result of this office action, no new charges are therefore incurred due to this office action.

SUMMARY

The invention teaches the deposition of a pattern of interconnecting lines and bond pads. Passivation layers are deposited over this metal pattern. A layer of photosensitive polyimide is deposited over the passivation layers. This layer of photosensitive polyimide is patterned, exposed and developed, the passivation layer is patterned and etched to expose the underlying bonding pads. The remaining polyimide is cured and

cross-linked and remains in place to serve as a buffer during further device packaging.

It is requested that should Examiner not find the claims to be allowable that he call the undersigned Attorney at his convenience at 845-452-5863 to overcome any problems preventing allowance.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned:

**"Version with markings to show changes made."**

Respectfully submitted,

Stephen B. Ackerman (Reg. No 37,761)

**Version with markings to show changes made**

IN THE SPECIFICATION

1) page 22, after the last paragraph please cancel the following matter:

[The invention, which provides a method for forming bonding pads of a semiconductor substrate, can be summarized as follows:

- top level interconnecting metal for interconnecting lines and top level bond pad metal for bond pads is provided, the interconnecting lines being adjacent to the top level bond pad, the interconnecting lines being adapted to ultra-small line spacing technologies, the top level metal being formed selectively on an insulating film overlying the main surface of a semiconductor substrate in which a desired circuit element is being formed, the surface of the insulating film being partially exposed
- a passivation layer is deposited over the top-level metal and over the partially exposed surface of the insulating layer, the passivation layer comprising a first and a second passivation layer

- a layer of photosensitive polyimide is deposited over the passivation layer, filling keyholes between closely spaced interconnect lines, thereby eliminating any detrimental effect caused by accumulation of semiconductor material inside the keyholes and eliminating negative effect that passivation layer imperfections have on device reliability, further preventing etching damage and damage of cracking and delamination to the surface of the passivation layer, further providing a stress buffer to the passivation layer, reducing stress impact on the passivation layer
- the layer of photosensitive polyimide is patterned and etched thereby forming a pattern for the bonding pads
- the passivation layer is patterned and etched thereby exposing the bond pad, the patterning and etching of the passivation layer to take place after the patterning and etching of the layer of photosensitive polyimide
- the photosensitive polyimide is cured and cross-linked, the curing and cross-linking of the photosensitive polyimide to take place after the patterning and etching of the passivation layer
- the thickness of the photosensitive polyimide is within the range of between 5.0 and 9.5 μm after deposition of the photosensitive polyimide whereby shrinkage of up to 40% of

the thickness can occur after curing of the layer of photosensitive polyimide, filling keyholes between closely spaced interconnect lines, thereby eliminating any detrimental effect caused by accumulation of semiconductor material inside the keyholes and eliminating negative effect that passivation layer imperfections have on device reliability, further preventing etching damage and damage of cracking and delamination to the surface of the passivation layer, further providing a stress buffer to the passivation layer, reducing stress impact on the passivation layer, allowing for adopting planarization technology to ultra-small line spacing technology

- specifically, the top level metal for interconnecting lines and top level metal for bond pads are formed within or on top of any layer of a semiconductor device other than or in addition to the semiconductor substrate, the interconnecting lines being adjacent to the bond pads, the interconnecting lines being adapted to ultra-small line spacing technologies, or
- the top level metal for interconnecting lines and top level metal for bond pads are formed selectively on the bare main surface of a semiconductor substrate in which a desired circuit element is being formed, the interconnecting lines

being adjacent to the top level metal for bond pads, the interconnecting lines being adapted to ultra-small line spacing technologies, or

- the top level metal for interconnecting lines and top level metal for bond pads are formed within or on top of any layer of a semiconductor device other than or in addition to the semiconductor substrate, or
- the top level metal for interconnecting lines and top level metal for bond pads are formed selectively on the bare main surface of a semiconductor
- further, the portion of the photosensitive polyimide that remains after completion of the patterning and etching the photosensitive polyimide is left in place to serve as a stress buffer and to provide protection against damage and extrusion of that portion of the surface of the passivation layer which is not removed by etching
- the patterning and etching the passivation layer is removing the passivation layer above and to the top metal of the bond pads, and
- additionally, a base layer of $SiO_2$ is created on the top surface of the substrate the base layer to be created prior to the creation of the top level metal thereby cushioning the

transition of stress between the silicon substrate and the wiring layer.]

[Alternatively the invention, which provides method of forming planarized bonding pads within the structure of a semiconductor device, can be summarized as follows:

- a semiconductor substrate is provided, the semiconductor substrate to contain electrical circuits or other electrical functional electrical components
- a wiring layer is provided having wiring and having a plurality of bond pads having a thickness, the wiring of the wiring layer being directly connected to the bond pads in addition to being connected to the electrical circuits or other electrical functional components within the semiconductor substrate, the wiring layer being adjacent to the plurality of bond pads, the wiring of the wiring layer being adapted to ultra-small line spacing technologies, the wiring layer being formed selectively on an insulating film overlying the main surface of a semiconductor substrate in which a desired circuit element is being formed, the surface of the insulating layer being partially exposed
- a layer of top metal is deposited over the bond pads, thereby depositing bond pad metal

- a passivation layer is deposited over the wiring layer and over the bond pad metal and over the exposed surface of the insulating layer
- a layer of photosensitive polyimide is deposited over the passivation layer to a thickness within the range of between 5.0 and 9.5 μm, filling keyholes between closely spaced wiring of the wiring layer, thereby eliminating any detrimental effect caused by accumulation of semiconductor material inside the keyholes and eliminating negative effect that passivation layer imperfections have on device reliability, further preventing etching damage and damage of cracking and delamination to the surface of the passivation layer, further providing a stress buffer to the passivation layer, reducing stress impact on the passivation layer
- the layer of photosensitive polyimide is patterned and etched, thereby forming a pattern of photosensitive polyimide, the pattern being identical to the pattern of the bond pads, partially removing the photosensitive polyimide from above the surface of the bond pads
- the layer of passivation is patterned and etched, thereby removing the passivation from above the bond pads, the patterning and etching of the passivation layer to take place

after the patterning and etching the layer of photosensitive polyimide, and

- the photosensitive polyimide is cured and cross-linked, thereby protecting the underlying circuitry, the curing and cross-linking of the photosensitive polyimide to take place after the etching of the passivation layer.]

IN THE CLAIMS

Please amend claim 1 as follows:

1. (Thrice Amended) A method for forming bonding pads of a semiconductor substrate comprising the steps of:

providing top level interconnecting metal for interconnecting lines and top level bond pad metal for bond pads, [said interconnecting lines being adjacent to said top level bond pad, said interconnecting lines being adapted to ultra-small line spacing technologies,] said top level metal being formed selectively on an insulating film overlying the main surface of a semiconductor substrate in which a desired circuit element is being formed, the surface of said insulating film being partially exposed;

depositing a passivation layer over said top-level metal and over the partially exposed surface of said insulating layer,

said passivation layer comprising a first and a second passivation layer;

depositing a layer of photosensitive polyimide over said passivation layer, filling keyholes between closely spaced interconnect lines, [thereby eliminating any detrimental effect caused by accumulation of semiconductor material inside said keyholes and eliminating negative effect that passivation layer imperfections have on device reliability, further] preventing etching damage and damage of cracking and delamination to the surface of said passivation layer, further providing a stress buffer to said passivation layer, reducing stress impact on the passivation layer;

patterning and etching said layer of photosensitive polyimide thereby forming a pattern for said bonding pads;

patterning and etching said passivation layer thereby exposing said bond pad, said patterning and etching of said passivation layer to take place after said patterning and etching of said layer of photosensitive polyimide; and

curing and cross-linking said photosensitive polyimide said curing and cross-linking of said photosensitive polyimide to take place after said patterning and etching of said passivation layer.

Please amend claim 8 as follows:

8. (Thrice Amended) The method of claim 1 wherein the thickness of said photosensitive polyimide is within the range of between 5.0 and 9.5 μm after deposition of said photosensitive polyimide whereby shrinkage of up to 40% of said thickness could occur after curing of said layer of photosensitive polyimide, filling keyholes between closely spaced interconnect lines, [thereby eliminating any detrimental effect caused by accumulation of semiconductor material inside said keyholes and eliminating negative effect that passivation layer imperfections have on device reliability, further] preventing etching damage and damage of cracking and delamination to the surface of said passivation layer, further providing a stress buffer to said passivation layer, reducing stress impact on the passivation layer[, allowing for adopting planarization technology to ultra-small line spacing technology].

Please amend claim 15 as follows:

15. (Thrice Amended) The method of claim 1 wherein said top level metal for interconnecting lines and top level metal for bond pads are formed within or on top of any layer of a semiconductor device other than or in addition to said semiconductor substrate[, said interconnecting lines being adjacent to said bond pads, said interconnecting lines being adapted to ultra-small line spacing technologies,].

Please amend claim 16 as follows:

16. (Thrice Amended) The method of claim 1 wherein said top level metal for interconnecting lines and top level metal for bond pads are formed selectively on the bare main surface of a semiconductor substrate in which a desired circuit element is being formed[, said interconnecting lines being adjacent to said top level metal for bond pads, said interconnecting lines being adapted to ultra-small line spacing technologies].

Please amend claim 17 as follows:

17. (Twice Amended) The method of claim 1 wherein said top level metal for interconnecting lines and top level metal for bond pads are formed within or on top of any layer of a semiconductor device other than or in addition to said semiconductor substrate[, said interconnecting lines being adjacent to said top level metal for bond pads, said interconnecting lines being adapted to ultra-small line spacing technologies].

Please amend claim 18 as follows:

18. (Twice Amended) The method of claim 1 wherein said top level metal for interconnecting lines and top level metal for bond pads are formed selectively on the bare main surface of a semiconductor[, said interconnecting lines being adjacent to

said top level metal for bond pads, said interconnecting lines being adapted to ultra-small line spacing technologies].

Please amend claim 20 as follows:

20. (Thrice Amended) A method of forming planarized bonding pads within the structure of a semiconductor device comprising the steps of:

providing a semiconductor substrate, said semiconductor substrate to contain electrical circuits or other electrical functional electrical components;

providing a wiring layer having wiring and having a plurality of bond pads having a thickness, the wiring of said wiring layer being directly connected to said bond pads in addition to being connected to said electrical circuits or other electrical functional components within said semiconductor substrate[, said wiring layer being adjacent to said plurality of bond pads, said wiring of said wiring layer being adapted to ultra-small line spacing technologies], the wiring layer being formed selectively on an insulating film overlying the main surface of a semiconductor substrate in which a desired circuit element is being formed, the surface of said insulating layer being partially exposed;

depositing a layer of top metal over said bond pads thereby depositing bond pad metal;

depositing a passivation layer over said wiring layer and over said bond pad metal and over the exposed surface of the insulating layer;

depositing a layer of photosensitive polyimide over said passivation layer to a thickness within the range of between 5.0 and 9.5 μm, filling keyholes between closely spaced wiring of said wiring layer, [thereby eliminating any detrimental effect caused by accumulation of semiconductor material inside said keyholes and eliminating negative effect that passivation layer imperfections have on device reliability, further] preventing etching damage and damage of cracking and delamination to the surface of said passivation layer, further providing a stress buffer to said passivation layer, reducing stress impact on the passivation layer;

patterning and etching said layer of photosensitive polyimide thereby forming a pattern of photosensitive polyimide, said pattern being identical to the pattern of said bond pads, partially removing said photosensitive polyimide from above the surface of said bond pads;

etching said layer of passivation, thereby removing said passivation from above said bond pads, said patterning and etching of said passivation layer to take place after said patterning and etching said layer of photosensitive polyimide; and

curing and cross-linking said photosensitive polyimide thereby protecting the underlying circuitry, said curing and cross-linking of said photosensitive polyimide to take place after said etching of said passivation layer.